CLAIM AMENDMENTS

The following is a complete listing of the pending claims:

1. (currently amended) A differential charge pump, comprising:

a current switch responsive to a pulse width difference between a differential up voltage and a differential down voltage to source and sink a current in a complementary fashion from a pair of differential output nodes, wherein the differential output nodes are voltage isolated from the current switch;

a first transconductance amplifier configured to convert a voltage at a first one of the differential output nodes into a first current; ~~and~~

a second transconductance amplifier configured to convert a voltage a second one of the differential output nodes into a second current that is complementary to the first current;

a resistive load coupled between a first node and a second node, wherein the first transconductance amplifier is configured to couple the first current to the first node and the second transconductance amplifier is configured to couple the second current to the second node;

a first differential pair of transistors biased by a first current source to conduct the current, the transistors in the first differential pair being responsive to the differential up voltage such that when the differential up voltage is pulsed the current is conducted by a first transistor in the first differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the first differential pair;

a second differential pair of transistors biased by a second current source to conduct the current such when the differential down voltage is pulsed the current is conducted by a first transistor in the second differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the second differential pair;

a first current source configured to source twice the current to a third node; and

a second current source configured to source twice the current to a fourth node, wherein the first transistor in the first differential pair and the second transistor in the second differential pair couples to the third node through a first pair of resistors, and wherein the second transistor in the first differential pair and the first transistor in the second differential couples to the fourth node through a second pair of resistors, whereby the first and second pairs of resistors perform the voltage isolation of the current switch from the differential output nodes.

2. (cancelled)

3. (cancelled)

4. (cancelled)

5. (cancelled)

6. (cancelled)

7. (currently amended) The charge pump of claim 1 ~~6~~, wherein the first and second transistors in the first and second differential pairs are NMOS transistors.

8. (currently amended) A differential phase-locked loop (PLL), comprising:

a phase detector configured to compare a feedback signal to a reference signal to produce a differential up voltage and a differential down voltage; and

a charge pump including a current switch responsive to a pulse width difference between the differential up voltage and the differential down voltage to source and sink a current in a complementary fashion from a pair of differential output nodes, wherein the differential output nodes are voltage isolated from the current switch, the charge pump including a common-mode feedback circuit configured so that the differential output nodes charge and discharge with respect to a common mode voltage, and wherein the common-mode feedback circuit is isolated from the differential output nodes through transconductance amplifiers;

wherein the charge pump includes a first differential pair of transistors biased by a first current source to conduct the current, the transistors in the first differential pair being responsive to the differential up voltage such that when the differential up voltage is pulsed the current is conducted by a first transistor in the first differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the first differential pair; and a

second differential pair of transistors biased by a second current source to conduct the current such when the differential down voltage is pulsed the current is conducted by a first transistor in the second differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the second differential pair;

and wherein the common-mode feedback circuit includes a first current source configured to source twice the current to a first node; and a second current source configured to source twice the current to a second node, wherein the first transistor in the first differential pair and the second transistor in the second differential pair couples to the first node through a first pair of resistors, and wherein the second transistor in the first differential pair and the first transistor in the second differential couples to the second node through a second pair of resistors, whereby the first and second pairs of resistors perform the voltage isolation of the current switch from the differential output nodes.

9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (currently amended) The differential PLL of claim 8 ~~12~~, wherein the transistors in the first and second differential pairs are NMOS transistors.

Claims 14 -- 19. (cancelled)

20. (new) The differential PLL of claim 12, further comprising:

a loop filter configured to filter voltages at the differential output nodes to provide a filtered differential output voltage;

a voltage-controlled oscillator configured to provide an output signal having a frequency dependent upon the filtered differential output voltage; and

a loop divider configured to divide the output signal to provide the feedback signal.